REMARKS

Applicant respectfully requests favorable reconsideration of this application for the reasons presented herein.

Applicant submits minor amendments for form, which Applicant respectfully submits do not raise new issues, do not necessitate further search by the Examiner, and do not require anything more than a cursory review by the Examiner to conclude that all claims stand in condition for allowance over the art relied upon by the Office Action.

The Office Action recites a rejection of claims 1-3, 5-21, 23-33 and 36 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,848,619 ("Leydier"). Office Action at pp. 3-12.

Applicant respectfully traverses, and submits that the rejections are in error.

Applicant's claim 1 includes, among other elements, "a processor; a charge storage device coupled to the processor; and

> a *current source* for supplying the processor with *substantially constant operating current* at multiple *nonzero current levels*, and adapted to vary its output *current* independently of an instantaneous power demand of the processor by switching, on at least one of a periodic and an aperiodic basis between the multiple nonzero *current levels (emphasis added)*

Claim 1, currently amended, at lines 2-7.

Illustrative example support for claim 1 is at Applicant's specification, page 3, lines 5-27, and at Applicant's Fig. 1. Referring to Applicant's Fig. 1, the depicted example includes current source 12 that supplies the processor 11 with current Icc,

and that current is substantially constant at any of multiple, for example, two different nonzero levels. Specification at p. 3, lines 5-7.

In contrast, *Leydier* discloses, an ON-OFF voltage source connecting to a load formed by capacitor CAP in parallel with a processor "uCE" and processor "uCL." The ON-OFF voltage source consists of the supply rail Vcc connecting to an ON-OFF switch "COM." This is not structure meeting the broadest reasonable meaning of the claim 1 language.

Leydier's structure *cannot* meet the claim 1 language because its switchable voltage source is *not* capable of performing the recited function of a current source providing substantially constant current at multiple different nonzero current levels.

First, *Leydier*'s ON-OFF switched supply is *not* a controllable *current* source. It is a *voltage* supply.

Second, *Leydier's* voltage supply, which is an ON-OFF switched supply, cannot output a *substantially constant* current at multiple non-zero value. More particularly, when Leydier's COM voltage supply switch closes, the switch's output current is an exponential RC decay, starting at a high initial value, then decaying toward the instantaneous current draw of the processors uCE uCL. *See Leydier* at Figs. 10A, 10B. *Leydier*'s OFF-ON COM voltage supply switch therefore outputs, based on simple RC equations, a series of exponential rise-decay waveforms. *See*

Leydier at Figs. 10B, 10C. Exponential rise-decay is not a "substantially constant" value.

Third, when *Leydier*'s COM switch opens, the current from *Leydier*'s COM voltage supply switch is necessarily *zero*. *Id*, at Figs. 10A, 10B. Applicant submits that zero is *not* a nonzero value.

Applicant respectfully submits, based on the reasons above, that a fair and objective reading of *Leydier*, for all that it discloses to a person of ordinary skill in the pertinent arts, shows that *Leydier* lacks subject matter meeting the broadest reasonable meaning of "a current supply ...substantially constant current ...at multiple different nonzero current levels."

Leydier therefore cannot anticipate Applicant's claim 1, or any of its dependent claims 2, 3, or 5-19.

Claim 20 is a method claim that includes subject matter substantially similar to claim 1 and, therefore, for at least the reasons Applicant presents for claim 1, Leydier cannot anticipate claim 20, or any of its dependent claims 21, 23-33 or 36.

With further respect to claim 3, the Office Action's position is that *Leydier* at col. 6, line 56, to col. 7, line 13; and at col. 8, lines 7-17, discloses "the current source ...switch[ing] between two different nonzero current levels." Office Action, at p. 3. The Office Action states a similar position on claim 21. *Id.*, at p. 8.

Applicant respectfully responds that the Office Action's position is in error. Applicant's claim 3 depends from claim 1, and claim 21 depends from claim 20.

Claims 1 and 20 recite a current source providing current to the processor. The cited sections of *Leydier,* however, describe *nothing* of a current source for a processor. The cited sections of *Leydier*, instead, describe a technology for the internal logic gates of the data processor itself. Applicant first submits that interpreting Applicant's claim 1 and 20 recital of "a current source for supplying" current *to* a processor to encompass *an internal logic gate* of the processor requires misinterpreting the recited language far beyond its broadest reasonable meaning.

Applicant further submits that the cited sections of *Leydier* have nothing to do with the subject matter of Applicant's invention. The cited sections of *Leydier* describe a purportedly inventive structure and operation of the logic gate that, when summed over the N logic gates (*see Leydier* at col. 7, line 5), the total consumption of energy is proportional to a supply voltage. This is not subject matter within the broadest reasonable meaning of the claim 3 and 21 language.

With further respect to claims 5 and 23, the Office Action's position is that *Leydier* at col. 6, line 56, through col. 7, line 13; and *Leydier* at col. 8, lines 7-17, teaches that "the interval between switching current levels is determined by an average power demand of the processor." *Id.*, at pp. 4, 8.

Applicant respectfully responds that the Office Action's position is in error; it departs from *Leydier's* disclosure, and/or is not consistent with the broadest reasonable meaning of the claim 5 and 23 language. First, *Leydier* lacks the base claim 1 and 20 current source. Second, the cited sections of *Leydier* describe the

"SMC" gate technology, and how the energy consumed by a particular logic gate does not, purportedly, exhibit information indicative of the logical operands. See Leydier, at col. 8, lines 54-67. This has nothing to so with the subject matter of claims 5 and 23.

With further respect to claims 6 and 24, the Office Action's position is that *Leydier* at col. 8, lines 54-67 ; and at col. 10, lines 19-21, discloses a second current source adapted to provide a noise current. *Id.*, at pp. 4, 8-9.

Applicant respectfully responds that the Office Action's positions on claims 6 and 24 are in error.

Claims 6 and 24 recite a second current source for supplying the processor. Applicant refers to Applicant's Fig. 1, showing example support with current supply 13 as one illustrative structure within the broadest reasonable meaning of claims 6 and 24. *Leydier*, in contrast, discloses no structure within the broadest reasonable meaning of claims 6 and 24. *Leydier* at col. 8, lines 54-67, instead discusses the current for the COM switch with respect to time. *Leydier* at col. 10, lines 19-21 discusses a pulse generator for controlling the COM switch. None of this embodies, or suggests toward, any subject matter that is within the broadest reasonable meaning of the claim 6 and 24 "second current source."

With further respect to claim 7, the Office Action takes the position that *Leydier*'s Abstract; and *Leydier* at col. 2. lines 27-60; and col. 4, lines 47-57, discloses

a control means adapted to maintain the supply voltage to the processor between an upper voltage limit and a lower voltage limit. *Id.*, at p. 4.

Applicant respectfully responds that the Office Action's position on claim 7 is in error. The claim 7 "control means" is a means-plus-function element under 35 U.S.C. § 112, ¶ 6. Applicant's disclosed structure for performing the function is a control 10 for the current source 12 feeding the capacitor C. Referring to Applicant's Fig. 3, this structure exploits the voltage across a capacitor being the integral, with respect to time, of the current through the capacitor. The result of the arrangement recited by claim 7is the Fig. 3 saw-tooth voltage ranging between the upper and lower value.

The cited sections of *Leydier*, in contrast, describe controlling its COM switch to its Vcc rail based on a single threshold value. This disclosed function is not with the broadest reasonable meaning of the claim 7 "control means" function, and this disclosed structure is not equivalent to Applicant's disclosed structure within 35 U.S.C. § 112, ¶ 6.

Leydier, for similar reasons, lacks the various subject matters recited by Applicant's claims 8, 9, 25 and 26.

With respect to Applicant's claim 10, the Office Action's position is that Leydier at col. 2, lines 28-60; and at col. 4, lines 2025, discloses the claimed "timer for determining a time period taken." Office Action at p. 5.

Applicant respectfully responds that the Office Action's position on claim 10 is in error.

Claim 10 recites a "timer." The cited sections of *Leydier* describe controlling the frequency of the COM switch clock based on the voltage across the processor. Applicant respectfully submits this is not subject matter within the broadest reasonable meaning of the word "timer" as it appears in claim 10.

With respect to Applicant's claims 11-16, 28-31, and 36, the Office Action's position is that *Leydier*, at the various sections cited by the Examiner, discloses the subject matter of each of these claims. Office Action at pp. 5-7 and 10-11.

Applicant respectfully responds that the Office Action's positions on these claims are in error. All are inconsistent with the broadest reasonable meaning of the claim language, and/or lack support in *Leydier*'s disclosure.

Applicant submits, first, that all of claims 11-16, 28-31, and 36 recite *controlling a current between a first and a second current level*. *Leydier*, in contrast, discloses nothing for supplying a *current level* to a processor, and much less controlling the level of a current to a processor.

Applicant submits, second, that all of these claims recite a *timer*, or determining a time for the processor voltage to move between limits. *Leydier* discloses *nothing* within the broadest reasonable meaning of a timer structure, or an act of timing.

Applicant submits, third, that all of these claims recite a timer, or determining a time for the processor voltage to move between *an upper and a lower limit*. *Leydier*, in contrast, discloses controlling the COM switch to the voltage rail Vcc based on a *single* threshold value.

With respect to claims 17 and 33, the Office Action's position is that *Leydier*, at col. 6, lines 19-25 and at Fig. 8, discloses a processor having an internal clock, the frequency of which is dependent upon the supply voltage to the processor. Office Action at pp. 5-7 and 10-11.

Applicant respectfully responds that the Office Action's positions on claims 17 and 33 are in error.

Leydier at col. 6, lines 19-25 discusses variation in the current through a logic gate with respect to changes in the voltage of the logical operands. This has nothing to do with the recital of claims 17 or 33. The cited sections of *Leydier* do not disclose or suggest subject matter that is within the broadest reasonable meaning of claims 17 or 33.

CONCLUSION

In view of the remarks above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. In the event that the fees submitted prove to be insufficient in connection with the filing of this paper, please charge our Deposit Account Number 50-0578 and please credit any excess fees to such Deposit Account. Should there be

any remaining issues that could be readily addressed over the telephone; the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-5256.

Respectfully submitted,
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